Linear Regression-Based Power Analysis for Digital Electronic Systems

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Abstract-This paper presents the linear regression-based power estimation technique uses the input patterns with the predefined characteristics. These patterns help to analyze the power consumption of the different intellectual-property (IP) cores in digital electronic systems. Our technique can accurately deals with combinational as well as sequential logic circuits at register-transfer level (RTL). Genetic algorithm (GA) is used for the generation of sequences with the statistical characteristics. During the power analysis procedure, the Monte Carlo simulation is performed and model function is extracted with the help of Look-Up-Table (LUT) approach. This function uses IPs primary inputs values for the analysis of power consumption. Our model demonstrates accurate and fast power estimation for IP-based digital system.

Keywords-Digital Systems, Power Estimation, Macro-Model, Input Metrics.

I. INTRODUCTION

Low-power consumption is nowadays very important design goal in very-large-scale integrated (VLSI) circuits. A key objective in low power-based system is to analyze power accurately. Power estimation at high design abstraction level, such as electronics and software engineering, is called for to facilitate new solutions to efficient power problems. Hence, a design and estimation approach for low-power is the key challenge to a successful System-on-chip (SoC) design. The rapid growth of transistor density and the operational frequency in digital electronic circuits have made power an important design constraint. Power optimization and estimation of SoC has nowadays become a difficult task for which the conventional approaches often prove to be inadequate. In order to handle the power, electronic design automation (EDA) tools have been introduced. These tools are very helpful for the minimizing of power dissipation in digital devices. The accurate power estimation EDA tools are needed from high to low abstraction levels.

In literature, there are several power analysis techniques for estimating the power consumption at different abstraction levels. Power estimation can be categorized in dynamic or static approaches at low level. Dynamic approaches are efficient and explicitly simulate the circuit with a typical input signal sequences. Statistical approaches such as Monte Carlo zero delay simulation [i] that helps the problem of input pattern dependencies. However, this technique assumes the transition activities and signal probabilities are independent and may therefore give inaccurate results. On the other side, static approaches do not simulate the design. Instead, they are dependent on the static knowledge (like correlations, switching-activities and signal-probabilities) about the input signal and estimate the same statistical properties for the internal circuit to measure the average power dissipation of the circuit. The input-dependence problem is faced by using selected statistical characteristics of the input patterns. These approaches are accurate and fast which can be obtained from large simulation results.

It is observed that the highest power optimization can be achieved at higher-level of the design abstractions. High level approaches can be roughly split into two types: bottom-to-up and top-to-down. The bottom-up approaches [ii-iv] are more accurate with the reused IP modules. In those modules, the internal details of the design are given and the power macro-model can be constructed easily with the power characterizations that are helpful in low to high level simulation estimates. In top-to-down techniques [v-vii] the design is specified without the technical information on the design implementation. Therefore these techniques are only helpful when the design was not previously implemented. However, they may not have accurate power analysis due to the insufficient information of the design implementation details.

RTL approaches [viii-ix] have been proposed to measure the switching activities of the design. These approaches are accurate but relatively slower and expensive, which limits the length of input streams. Power consumption in digit electronic systems are input pattern dependent. To measure accurate power dissipation, set characteristics of input samples are needed. Usually these input samples have large sample size. If samples are selected arbitrarily, may not be able to measure the expected behavior of the power dissipation of the circuit. To handle this important problem, vector compaction approach was introduced in [x]. This approach was used in input patterns into a

Stimulus sequence which has smaller size. These approaches are more accurate but they can not efficiently considered factors like propagation delay, glitch-generation etc. RTL power macro-modeling technique was developed with the variety of equations and Look-Up-Table based approaches. Among those, building power macro-model for the digital system was popular technique for analysis of the average power dissipation. In the literature survey, most power model increases in complexity to capture the accuracy requirements. To reduce the simulation time, input sample compaction technique was introduced that captures the exact power behavior of the circuit.

In this work, we used our research in [xi-xiv] developing for the low-power modeling approaches in the power estimation method for more complex digital test system. Our proposed power model in this paper is the linear regression-based LUT approach at RTL. We use genetic algorithm to investigate the statistical properties of the input sample streams that influences power consumption of digital system. The average input statistical characteristics of our model are the transition-density '*TD'*, signal-probability *'SP'*, spatial-correlation '*SC'* and temporal-correlation '*TC'*. We use IP-based macro-modules for our experiments and achieve comparatively good accuracy.

The paper is organized as follows: Initially we give the brief problem statement and we discuss the introductory background of our linear regression-based power analysis method. Then we explore our GA algorithm and the model is evaluated in experimental results. Finally, we summarizes our work.

II. Problem Statement

The problem solved in this paper is to find a statistical method which accurately and fast estimates the power consumption in any digital system by the addition of its each IP-module. This method makes the power analysis of digital system an easy task that helps for the analysis of power features at higher level.

III. Linear Regression-based Power Analysis

The flow of our high-level power macro-modeling method is shown in figure 1. Our approach consists of the following steps:

1) Characterization of each IP module at high-level design library by simulating it under pseudo random signals and fit statistical variables regression curve to the power dissipation results using a least-mean-square (LMS) error fit.
2) Extractions of the power function from parameter model of IPs with using Monte Carlo simulation approach. The high-level simulator is used to collect power values for various IP modules in the SoC System.
3) Evaluation of the power macro-model function at high-level IP design which are found in the library by plugging the parameter values in the corresponding macro-model function.

The proposed model is linear regression-based LUT approach. To obtain power macro-model, a linear function is used in (1) that estimates power of the given input vector streams.

$$P_{IP_{avg}} = \beta_0 + \beta_1.\alpha_1 + \beta_2.\alpha_2 + \ldots + \beta_{n-1}.\alpha_{n-1} + \beta_n.\alpha_n + \varepsilon \quad (1)$$

Where P_{IP_avg} is the average power dissipation of the individual IP core, $\beta_0, \beta_1, \ldots \beta_{n-1}, \beta_n$ are the regression coefficients obtained from the regression analysis, $\alpha_1, \alpha_2, \ldots, \alpha_{n-1}, \alpha_n$ are the statistical characteristics of each input and ϵ is the error. The parameters of the regression are determined using the linear regression by finding the least-square fit. Equation (1) can be expressed in (2):

$$P_{IP_{avg}} = \beta_0 + \beta_1.TD + \beta_2.SP + \beta_3.SC + \beta_4.TC + \varepsilon \quad (2)$$

where *TD, SP, SC, TC* are the statistical characteristics of our model.

The regression equation in (2) can be computed by applying the set defined input pattern values of *TD, SP, SC,* and *TC*. The determination coefficient p^2 is measured to improve the quality of (2). It determines the proportionality of data set patterns of the input characteristics that helps to predict the accurate power. p^2 varies from 0 to1 and it is defined in (3):

$$p^2 = 1 - \frac{\epsilon_s}{r} \quad (3)$$

Where ϵ_S and r is defined in (4) and (5):

$$\epsilon_s = \sum(x_i - y_i)^2 \quad (4)$$

$$r = \sum(x_i - \bar{x})^2 \quad (5)$$

With $\bar{x}$ is the mean of the estimated data, x_i predicts the values and y_i is the data set value.

The proposed signal generation algorithm generates input streams of different values with the characterizations of *TD, SP, SC,* and *TC*. These values with different combination stored in LUT that allows the power analysis with minimum error. It measures the average power dissipation P_{IP_Module} in (6).

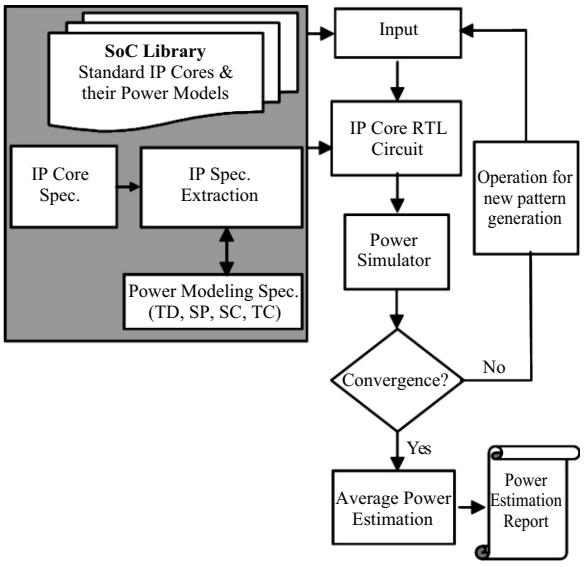

Fig. 1. Power estimation methodology.

$$P_{IP\_Module} = f\ (TD, SP, SC, TC) \quad (6)$$

The *f(.)* is a mapping-method to be performed during the characterization of the input characteristics. To find function *f(.)*, we must sample a set number of streams with several *TD, SP, SC,*and *TC* values. The power dissipation of IP modules-based system P_{IP_Module} is obtained in (7) using (6).

$$P_{IP\_System} = \sum_{i=1}^{n} P_{IPi\_Module} \quad (7)$$

In this technique, the pattern of input singles are generated according to the input statistical properties (*TD, SP, SC,*and *TC)* and power dissipation P_{IP_Module} is predicted in (6). Then Monte-Carlo zero delay method [viii] is used with several input streams of their statistical knowledge and evaluated the accuracy of P_{IP_Module}. The accuracy of the model on each module requires information of the statistical signals. While maintaining accuracy to obtain this knowledge, several simulations are performed with various values of *TD, SP, SC,* and *TC* of each IP module. In Fig. 2, the inputs of the module *IP-M* are the inputs of the IP-based digital system and outputs of *IP-M* are inputs of $IP\text{-}M_{1a}$, $IP\text{-}M_{1b}$, $IP\text{-}M_{1c}$, and $IP\text{-}M_{1d}$, and continues till the final outputs. The output statistical characteristic values for each IP module can be used as input signal statistical values of the related connected IP modules. For *IP-M* module, we generate random signals of several different patterns of *TD, SP, SC,* and *TC*. Then to build LUT, we performed several simulations in our test system. For each module different values of average input statistical properties are predicted by using large simulations. The different values of the system's power dissipation are determined using power simulator. The simulated power is compared by using HSPICE simulator with estimated power model P_{IP_System} in (7).

IV. Algorithm Exploration

Genetic algorithm generates randomly input sequences of *TD, SP, SC,* and *TC* for the power estimation of IP-based test system. Finding the optimal solution that satisfies the convergence criteria of the power waveforms during simulations of the system is the main purpose of power estimation. Our GA procedure is as follows:

1. Generate an initial population P_i, and then set p_{cross} and p_{mut} which are crossover and mutation probabilities respectively. Where $p_{cross} \in (0,1)$ and $p_{mut} \in (0,1)$. Set the generation counter with $counter\_t := 1$.
2. Evaluate the fitness function value F for all possible chromosomes in P_{chrom} with the selection of an intermediate population P'_{chrom} from the possible current population P_{chrom}.
3. Generation of random number from (0,1) with every chromosome in P'_{chrom}, then add to evolve each chromosome to the parent set PS_{chrom}, if

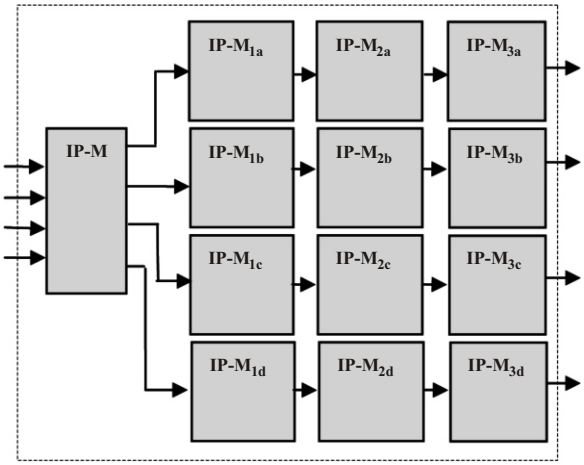

Fig. 2. IP-based test system

related number is less than p_{cross}. Following steps must repeat until all parents in PS_{chrom} are mutually mated: (a). Select two parents p_a and p_b from PS_{chrom}. Mate p_a and p_b to regenerate children c_a and c_b. (b). The children pool set PS_{child} updating through $PS_{child} := PS_{child} \cup \{c_a, c_b\}$ and $PS_{chrom} := PS_{chrom} - \{p_a, p_b\}$

4. Associated random number generation from (0,1) for all possible gene in every chromosome in P'_{chrom}. Then mutation of this gene is performed, if the associated number is less than p_{mut} and further add the mutated chromosome only with the children pool set PS_{child}.
5. Finally, if the stopping criteria is satisfactory, then terminate the population generation. Else the selection for the next generation $P_{chrom+1}$ from $P_{chrom} \cup PS_{child}$. Set $PS_{child} := \{\}$, set

counter_t := *counter_t* + 1, and go to the step 2.

V. Experimental Results

In experimental results, we discuss our accurate technique for IP-based test system is shown in Fig. 2. We have developed this technique and build the power macro-model at architectural abstraction level. Accuracy of genetic algorithm is implemented on IP-based macro-modules. For these modules, random input pattern is generated for several *TD, SP, SC,* and *TC* values. The input pattern generation of our new technique is highly auto-correlated. The power consumption is measured by using Monte Carlo zero delay method. Several values are predicted by LUT based approach and these power values are compared with simulation results. Finally, we performed different error analysis to compare our macro-model results with the commercial tool. The maximum, minimum, average and root mean square (rms) errors are computed using (8) and (9).

$$\varepsilon_{rms} = \frac{1}{n}\sum_{i=0}^{n}\sqrt{\left(\frac{P_{sim_i} - P_{est_i}}{P_{est_i}}\right)^2} \quad (8)$$

$$\varepsilon_{avg} = \frac{\sum_{i=0}^{n} P_{sim_i} - \sum_{i=0}^{n} P_{est_i}}{\sum_{i=0}^{n} P_{est_i}} \quad (9)$$

Where P_{sim} and P_{est} are the simulated and estimated powers respectively.

The results demonstrated that the proposed GA can generate random patterns with high convergence and produce accurate statistical values. For the input pattern characterizations of *TD, SP, SC,* and *TC* we select the probabilistic range of [0, 1]. Our algorithm generated 740 different input streams with width of 8, 16 and 32-bits. The signal stream length is 4000 for macro-module. Analysis of convergence on power may help us to find the simulation interval, by determining when the power value is more close to the appropriate interval length in the steady state waveform. The sequence generator has high value of convergence and uniformity. The appropriate length is found 3650 for the test system. The warm up interval is close to 550 and the steady state interval is obtained 2050.

The power dissipation is observed of *IP-*M_{1a}, *IP-*M_{1b}, *IP-*M_{1c}, and *IP-*M_{1d}, modules with different input characteristic values. The result demonstrates that among other characteristics, the transition activity *TD* is more important for the power consumption. The power and *TD* are considerable linear with each other. The input correlation factors *TD* and *SC* are not very effective with the power and not very sensitive as compared to *TD*. To fit the coefficient's in the model, regression method is obtained. For several modules, the coefficient of correlation is estimated about 94%.

The selected number of the input signals and the estimate values error obtained with our macro-model function is shown in table 1 and Fig. 3. From Table I that *f(.)* in (6) is more accurate enough for estimating the average power consumption for IP-based test module. Columns two, three, four and five gives the minimum, maximum, average and rms-errors for the estimates used with our IP-based macro model. HSPICE have been used as power simulator in our power estimation procedure. In experiments, we computed the average minimum error 1.65%, average maximum error 3.49%, average error 2.70% and average rms error 5.93%. Our results demonstrated that our approach can be used to achieve accurate and fast power estimates in the early stage of digital system design. For the entire test system with interconnects/wires the error increases by 12-20%. This error can be improved by implementing different techniques that deal with the data path of interconnects/wires with IP macro-modules. The average error of the entire IP-based test system is 7.15%. The reference results of the system's power dissipation are determined using commercial power simulator. The table illustrates the function has less accuracy in some cases than others. We have found in a given specified range of statistical characteristic values between [0.3-0.7] is more accurate and comparatively less accurate between [0-0.3] and [0.7-1]. The experimental result shows that *TD* is more dominant factor for power dissipation in the test system and normally proportional to the power measurements. The correlation factors are not very effective to power dissipation and are significantly not more sensitive than the switching density. The number of input/output (I/O) is important to the (I/O) characteristics for the system.

TABLE I
Power Estimation Accuracy

Test System	εmin	εmax	εavg	εrms
IP - M	1.32%	3.58%	2.16%	6.54%
IP - M_{1a}	2.13%	4.87%	3.64%	7.33%
IP - M_{1b}	2.45%	5.56%	4.43%	8.43%
IP - M_{1c}	2.50%	4.98%	3.68%	6.89%
IP - M_{1d}	2.76%	4.90%	4.61%	8.38%
IP - M_{2a}	1.34%	3.43%	2.28%	5.56%
IP - M_{2b}	0.60%	1.45%	1.19%	4.32%
IP - M_{2c}	0.75%	2.45%	1.34%	4.12%
IP - M_{2d}	1.45%	4.32%	2.56%	5.78%
IP - M_{3a}	1.89%	2.90%	2.46%	5.14%
IP - M_{3b}	1.08%	1.89%	1.42%	3.97%
IP - M_{3c}	1.50%	2.70%	3.01%	4.58%
IP - M_{3d}	1.76%	2.32%	2.42%	6.15%
Average	**1.6%**	**3.4%**	**2.70%**	**5.93%**

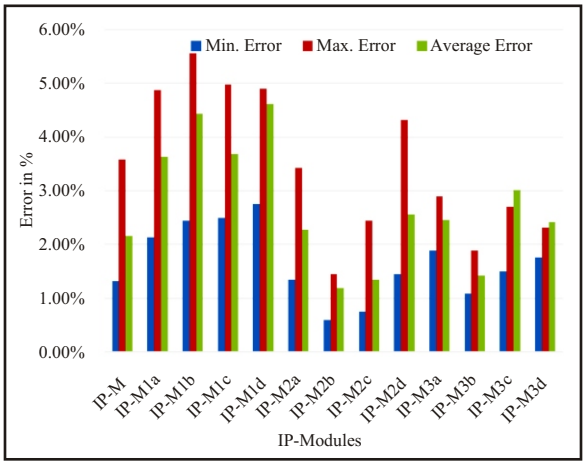

Fig. 3. Error analysis of IP-modules in digital system

VI. Conclusions

The presented work is an accurate simulation-based power analysis technique at the architectural level implemented on IP test system. In this work, for each IP module, we measure just 2.70% average and 5.93% rms errors respectively. But for whole test system with interconnects, the average error is found 7.15% and a correlation coefficient is observed around 94%. The results showed the accuracy has been improved in some cases than in others. Nowadays, we are using complex systems for evaluating this model and making it more accurate as compared to other models in this area.

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